				ATTY DOCKET NO.	I I			
ID	_				TO.0539D1US (P10144D) 10/652,631			
0 1 T		MATION DISCLOSUR			APPLICANT(S): CHARLES DENNISON			
62 2	ילי און	se several sheets if ned	essary)	FILING DATE:				
MOV 0 3 2	ادی ادی	<u> </u>		August 29, 2003				
S.	25/		U.S. F	ATENT DOCUMENTS				·=
EXAMINER)		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	Ā.							
	B.							
	C.						 	
	D.							
	L		FOREIG	N PATENT DOCUMENTS				
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES YES	LATION NO
	E.							
	F.							
	G.	·						
	H.							
	1	OTHER DOCU	MENTS (Inclu	ding Author, Title, Date, Pert	inent Pages, E	tc.)		
M	1.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Jeong, U.I., Jeong, H.S. and Kim, Kinam, "Completely CMOS-Compatible Phase-Change Nonvolatile RAM Using NMOS Cell Transistors," presented at 2003 19th IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, California, February 26-20, 2003						
	J.	Ha, Y.H., Yi, J.H., Horii, H., Park, J.H., Joo, S.H., Park, S.O., Chung, U-In and Moon, J.T., "An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003						
	K.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Oh, J.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Chung, U.I., Jeong, H.S. and Kim, Kinam, "Full Integration and Reliability Evaluation of Phase-change RAM Based on 0.24 mm-CMOS Technologies," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003						
L. Horii, H., Yi, J.H., Park, J.H., Ha, Y.H., Baek, I.G., Park, S.O., Hwang, Y.N., Lee, S.H., Kim, Y.T., Lee K.H., Chung, U-In and Moon, J.T., "A Novel Cell Technology Using N-doped GeSbTe Films for Phase Change RAM," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003								se
	M.							
	N.							
	0.							
EXAMINER	12	- I	- 	DATE CONSIDERED	5/20	4		
*EXAMINER:	Initial if n	eference considered, whether or r	ot citation is in confor	mance with MPEP 609; Draw line through c			sidered. Inc	dude copy
of this form w PTO-1449	ith next oo	ommunication to applicant.					Pa	ge 1 of 1